

**(19) World Intellectual Property
Organization
International Bureau**



(43) International Publication Date
8 January 2004 (08.01.2004)

(10) International Publication Number
WO 2004/003970 A2

(51) International Patent Classification⁷: **H01L**

(21) International Application Number: **PCT/US2003/019085**

(22) International Filing Date: **18 June 2003 (18.06.2003)**

(25) Filing Language: **English**

(26) Publication Language: **English**

(30) Priority Data:

60/392,023	26 June 2002 (26.06.2002)	US
60/391,802	26 June 2002 (26.06.2002)	US

(71) Applicant (*for all designated States except US*): **SEME-QUIP INC.** [US/US]; 34 Sullivan Road, Unit 21, Billerica, MA 01862 (US).

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **KRULL, Wade, A.** [US/US]; 8 Smith Street, Marblehead, MA 01945 (US). **JACOBSON, Dale, C.** [US/US]; 16 Flintlock Road, Salem, NH 03079 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

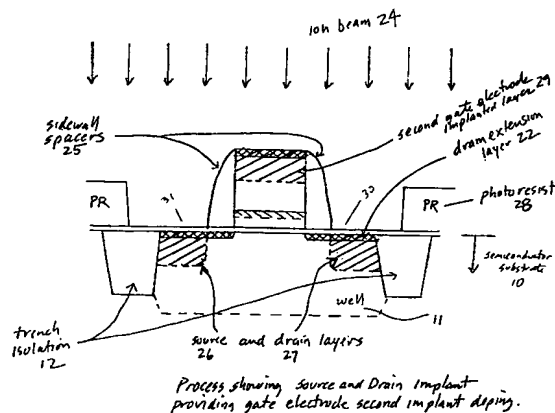
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING A SEMICONDUCTOR DEVICE



(57) Abstract: A method is proposed for the fabrication of the gate electrode of a semiconductor device such that the effects of gate depletion are minimized. The method is comprised of a dual deposition process wherein the first step is a very thin layer that is doped very heavily by ion implantation. The second deposition, with an associated ion implant for doping, completes the gate electrode. With the two-deposition process, it is possible to maximize the doping at the gate electrode/gate dielectric interface while minimizing risk of boron penetration of the gate dielectric. A further development of this method includes the patterning of both gate electrode layers with the advantage of utilizing the drain extension and source/drain implants as the gate doping implants and the option of offsetting the two patterns to create an asymmetric device. A method is also provided for the formation of shallow junctions in a semiconductor substrate by diffusion of dopant from an implanted layer contained within a dielectric layer into the semiconductor surface. Further, the ion implanted layer is provided with a second implanted species, such as hydrogen, in addition to the intended dopant species, wherein said species enhances the diffusivity of the dopant in the dielectric layer.